

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 7,

Lines 30-47, claim 1 should read as follows:

- 1. A method for storing data by accumulating charges in a capacitor, comprising:
lowering a potential of a first bit line of a pair of bit lines to a level within a range that prevents data in a memory cell from being lost; and
making a short circuit between said pair of bit lines to perform a precharge of said pair of bit lines by bringing the potential of said pair of bit lines to an intermediate potential,
wherein said short circuit is made after said lowering occurs. --.

Column 7, lines 48-67 to Column 8, lines 1-3, change claim 2 as follows:

- 2. A semiconductor memory apparatus for storing data by accumulating charges in a capacitor, comprising:
a forced step-down circuit comprising a first switching element having one end connected to a driving line on the high side,
a forced step-down capacitor and a second switching element arranged in parallel between the other end of the first switching element and a ground potential, and
a pair of bit lines, wherein a first bit line of said pair of bit lines is connected to said driving line, wherein
the second switching element is brought into an on state to hold the forced step-down capacitor at zero potential before the first switching element is brought into an on state, and
before making a short circuit in the pair of bit lines to perform a precharge by bringing a potential of a pair of bit lines to an intermediate potential, the first switching element is brought into an on state to lower a potential of the driving line on the high side to a level within a range that prevents data written in a memory cell from being lost. --.

Signed and Sealed this

Twenty-first Day of March, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office